

**METHOD AND SYSTEM TO COMPENSATE FOR SCANNER SYSTEM
TIMING VARIABILITY IN A SEMICONDUCTOR
WAFER FABRICATION SYSTEM**

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FIELD OF THE INVENTION

The invention relates generally to semiconductor wafer fabrication systems that comprise a track system and a scanner system, and more specifically to compensating such wafer fabrication systems for deviations from nominal timing in the scanner system.

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BACKGROUND OF THE INVENTION

Modern integrated circuits (ICs) are fabricated on semiconductor wafers that are mass produced in fabrication sites. The fabrications sites (or "fabs") employ various types of automatic equipment that must function to very
15 exacting and carefully controlled operating parameters. Fig. 1 depicts some of the process steps or modules found in a generic fab system 10. System 10 may be thought of as a track system 20 that comprises a variety of production modules, and a scanner (or stepper) system 30. Track system 20 typically operates synchronously under control of a computer system 40 that, among
20 other tasks, outputs a track system clock signal (TRACK CLOCK). By synchronously it is meant that wafers are moved in the track system 20 responsive to the track clock signal.

The wafers under production are made available for input to the scanner
25 system 30 responsive to the track clock signal. However scanner system 30 receives the wafers and outputs scanner system-completed wafers responsive to its internal scanner system clock (SCANNER CLOCK).

Understandably much attention is given in the prior art to trying to synchronize the track clock and the scanner clock to reduce dead-time in moving and
30 processing wafers through the overall fabrication system. But to achieve good synchronization between the track clock and the scanner clock, the

timing in the scanner system must exhibit a substantially consistent periodicity. But in practice, exposure procedures within the scanner system can exhibit a timing deviation from nominal periodicity, which deviation or variability hampers clock synchronization.

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Exemplary modules within track system 20 are shown in Fig. 1. At the upper left region of Fig. 1, a sequence of wafers are input to system 20. A chill plate module 50 typically is used to stabilize the wafer temperature by about 1°C to room temperature before the wafers enter a spin coater 60 where a film of polymer photoresist is placed on the upper surface of the wafer. In some processes, at step 60 an anti-reflection coating may first be deposited upon the upper wafer surface and the wafer then baked (e.g., module or step 70) and then returned to the spin coater 60 for deposition of photo resist. As modern photolithography seeks to define smaller and smaller feature size using shorter wavelength light, ultraviolet reflectivity becomes a greater problem, and thus the use of anti-reflection layer(s).

Eventually the wafer is passed by a robotic unit 140 to a bake plate 70 where the film of photoresist is hardened and excess solvents are driven out of the wafer with heat. A subsequent chill plate process 80 cools the wafers to a stabilized room temperature. Upon receipt of a track clock signal issued by computer system 40, the wafer under process is then sent out of the thus-described portion of track system 20 and is available for input to the stepper/scanner system 30. Stepper/scanner system 30 will accept the wafer in question responsive to a signal from the scanner clock. Within system 30 various lithographic techniques may be carried out upon the wafer in question. At module or step 90, the wafer is subjected to a post-exposure bake (PEB), using a PEB bake plate, and then to a chill plate 100, that returns the wafer to a stabilized ambient room temperature. A developer module stage 110 typically follows, during which the latent lithographic image that was formed within the stepper/scanner module 30 is developed in the polymer film on the

wafer upper surface. In a positive tone image, the portions of the photoresist exposed to light will become soluble and dissolve away in solution to expose desired regions of the wafer structure. A bake plate step 120 follows to dry and harden the wafer surface. An etcher module 130 then follows, and the thus-processed wafer is returned to a chill plate, e.g., module 50. Several of the steps or stages shown in Fig. 1 may be repeated for the same wafer dozens of time, depending upon the specifics of the processes involved (e.g., the "recipe". Typically devices shown generically as robotic arms 140 may be used to mechanically move wafers from one module to another.

In practice the rate at which track system 20 can send wafers for input to stepper/scanner system 30 may not coincide with the rate at which stepper/scanner system 30 is ready to receive ("R2R") new wafers. Similarly, the time when scanner system 30 is ready to send ("R2S") wafers back into track system 20 may not coincide with the moment at which track system 20 is ready to receive wafers for further processing. In some prior art systems 10, buffers such as 150 may be included to add time to processing of wafers within system 20. One or more buffers or buffer functions may be used in system 10 to absorb what would otherwise be disturbances to the time flow of wafers. A buffer may be a physical entity, for example a module used as a temporary storage site to hold excess wafers longer than needed for processing at that station, perhaps a dedicated buffer station, or a robotic arm temporarily used as a storage site for wafers.

By way of example, assume that responsive to timing of the track clock signal chill plate 80 is ready to send wafers into the stepper/scanner system 30 sooner than the stepper/scanner clock allows system 30 to be ready. When it is known that stepper/scanner system 30 is ready to receive wafers, the robotic arm 140 can load wafers into system 30, taking them if necessary from a buffer 150.

Understandably having to provide extra robotic arms and/or buffers to try to improve the output timing of track system 20 is not an optimum solution to the problem of enabling a better timing match between system 20 and system 30. There can be time conflicts within system 10 between modules competing for
5 access to a given module, and it can be necessary to try to force time matching between wafers sent out of system 20, and wafers received into system 30, and then wafers exiting system 30 back into track system 20. But providing buffers 150 and/or additional robotic type mechanisms 140 to try to smooth out system flow requires additional cost and additional floor space
10 within the fab, and will actually reduce wafer throughput.

One prior art solution to helping resolve resource conflicts within track system 20 is described in U.S. patent no. 6,418,356 (July 2002) to H. Oh, inventor herein. In the '356 patent, conflicts for transportation resources (e.g., robotic
15 mechanism) are resolved by selectively adding "wait" time to modules that can tolerate such wait states without substantially degrading on-wafer production results associated with track system 20. Applicant incorporates herein by reference U.S. patent no. 6,418,356.

20 But even if track system resource conflicts can be resolved, deviations from nominal timing in the associated scanner system can degrade overall fabrication system performance. What is needed is a method of compensating for such scanner system timing deviations such that the timing match between the ready to send (R2S) state of the track system and the
25 ready to receive (R2R) state of the stepper/scanner lithographic system is maintained.

The present invention provides such compensation for time deviations in a scanner system.

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SUMMARY OF THE PRESENT INVENTION

The present invention operates a semiconductor wafer fabrication system that includes a track system and a scanner system such that deviations from anticipated nominal timing in the scanner system are compensated for. Such time deviations typically arise from variations in scanner system exposure

5 times. The present invention detects such scanner system time deviations and dynamically inserts additional time "delays" into the wafer production system to help compensate therefor, and to thus preserve good synchronization of wafer flow across the track system to scanner system interface.

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These dynamically inserted delays are in addition to pre-planned "waits" that are added into the wafer production recipe at non-critical module phases of the process, as disclosed in U.S. patent no. 6,418,356. The resultant semiconductor wafer fabrication system can maintain a synchronized wafer

15 flow, and thus achieve improved throughput.

Other features and advantages of the invention will appear from the following description in which the preferred embodiments have been set forth in detail, in conjunction with their accompanying drawings.

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BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing exemplary modules or processes in a two-clock semiconductor wafer production system operating without scanner system timing compensation, according to the prior art;

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FIG. 2 is a block diagram showing exemplary modules or processes in a semiconductor wafer production system with scanner system timing compensation, according to the present invention;

FIG. 3, comprising FIGS. 3A and 3B, is a flow chart depicting the process flow for twenty-five wafers produced according to the exemplary recipe of Table 1, according to the present invention; and

- 5 FIG. 4, comprising FIGS. 4A-4F, is a spreadsheet depicting data for the wafer flow shown in Figs. 3A and 3B, according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

- Fig. 2 is a block diagram of a semiconductor wafer production system 200 that
10 includes a track system 20' and a scanner system 30'. Systems 20' and 30' may be the same as systems 20 and 30 in Fig. 1, or may include different and/or different numbers of modules and more or less robotic units.

- It may be assumed that system 200 has track system 20' compensation in the
15 form of inserted "wait" times as described in U.S. patent no. 6,418,356. However in contrast to what is described in the '356 patent, track system 20' advantageously also has compensation against deviations from nominal scanner system timing, which is to say, deviations from nominal scanner system clock periodicity. Such compensation is in the form of inserted time
20 "delays".

- System 200 preferably operates under control of computer system 210 whose computer readable memory stores (or can be loaded with) software 220 that when executed by the computer CPU implements the above system
25 operation. Computer system 210 can readily compare actual scanner system 30' clock timing against a nominal clock timing to detect deviations in periodicity from nominal. When such timing deviations are detected, software 210 upon CPU execution causes the insertion into track system 20' of appropriate time "delays" (as contrasted with the insertion of '356 patent pre-
30 planned "waits", which are introduced into the wafer production recipe even before system 200 is turned-on). As described herein, such inserted "delays"

improve the match between timing of wafers sent by track system 20' and timing of wafers received by scanner system 30', e.g., wafers sent from chill plate 80 into scanner system 30', as well as wafers sent from scanner system 30' into post-exposure bake module 90 in track system 20', in exemplary Fig.

5 2.

Track system 20' is shown with four robotic stations: LRP-230 (or "LPR") is a load port robotic unit associated with loading wafers into/out of system 200, CTR-230 (or "CTR") is a robotic unit associated with coater module 60, SIR-230 (or "SIR") is a robot associated loading wafers into and out of scanner system 30', and DVR-230 (or "DVR") , a robot associated generally with developer module 110. All four robotic units LRP, CTR, SIR, and DVR preferably have two arms, such as robotic units developed by assignee ASML, Inc. While system 200 will be described with reference to these four robotic stations, it is understood that the present invention may be practiced with wafer production systems employing fewer or more than four track system robotic stations, or with systems not employing any dual-armed robotic stations.

20 Table 1 below will now be described with reference to the present invention. In Table 1, rows 11-15 (shown with shading) denote process steps associated with scanner system 30'; the remaining process steps are associated with track system 20'. Nominally a period of 40.0 seconds is assumed for the wafer recipe given in Table 1, e.g., in the nominal case a new wafer enters the system for processing every 40 seconds.

TABLE 1

Process Step	Robot Assignment		Transport Time	Process +OH Time	Planned Wait
	Pick By:	Move Type			
LPx	LPR	Sngl	7.0	0.00	0.00
CP1x	CTR	Sngl	7.0	24.00	20.00
BARCx	CTR	Swap	5.5	44.00	33.50

HP1x	LPR	Sngl	7.0	64.00	0.00
CP4x	LPR	Swap	5.5	84.00	35.00
CP1x	CTR	Sngl	7.0	84.00	42.00
CTx	CTR	Swap	5.5	49.00	28.50
HP2x	SIR	Sngl	7.0	94.00	0.00
CP2x	SIR	Swap	5.5	64.00	13.50
OEBRx	SIR	Swap	8.0	34.00	5.00
IN-PED	WHR	Sngl	12.5	1.00	0.00
ALIGN	DIR	Sngl	6.5	19.30	25.00
EXPOSE	DIR	Swap	6.5	33.50	0.00
DISCHRG	WHR	Sngl	12.4	1.00	0.00
OUT-PED	SIR	SWAP	9.5	1.00	0.00
HP3x	DVR	Sngl	7.0	94.00	0.00
CP3x	DVR	Swap	5.5	64.00	13.50
DEVx	DVR	Swap	5.5	89.00	30.00
CP4x	LPR	Sngl	7.0	5.00	31.00
LPx			0.0	0.00	0.00

Referring to Table 1, the first column denotes process steps, and the fifth column denotes the process and overhead (OH) time corresponding to the process step. By way of example, in a chill plate operation (e.g., CP1x), the overhead time refers to the time necessary to open and close the chill plate chamber module, whereas the process time represents the actual duration of a timed-chill within the closed chill plate chamber.

Thus in Table 1, the first column represents modules for the process steps, where LPx denotes load port, CP1x, CP2x, CP3x denote chill plates (e.g., perhaps chill plates 50, 80, 100 in Fig. 2), BARCx denotes bottom anti-reflection coating module (e.g., a step carried out by spin coater module 60), HP1x, HP2x, HP3x, HP4x denote hot or bake plates (e.g., bake plates 70, 90, 120 in Fig. 2), CTx denotes a coater module (e.g., module 60 in Fig. 2), OEBRx denotes removal of the bead formed on the outer edge of a wafer. IN-PED and OUT-PED denote input and output pedestals within scanner system 30', ALIGN denotes wafer alignment within scanner system 30',

EXPOSE refers to wafer exposure within scanner system 30, and DISCHARGE refers to a discharge chute within scanner system 30'. The five rows of data in Table 1 relating to scanner system 30' are shown with background shading and dark borders; the remaining rows of data represent steps in track system 20'.

Columns two and three in Table 1 denote robot assignments in the exemplary embodiment to be described and robotic movements. LPR denotes load port robot (e.g., LPR-230 in Fig. 2), CTR denotes coater robot (e.g., CTR-230 in Fig. 2), SIR denotes a stepper interface robot (e.g., SIR-230 in Fig. 2), WHR and DIR denote a wafer handling robots associated with scanner system 30' (e.g., WHR-240, DHR-240 in Fig. 2). In a so-called single movement, a generic robot that must move a wafer from a first process module to a following second process module must first remove the wafer already in the second process module before relocating the first wafer to the second process module. In a swap movement, a two-armed robotic mechanism is used in which the first robot arm can pick up a first wafer from a first module, and a second wafer from a second module, and then use the first arm to position the first wafer in the second module. Where feasible, swap movements are preferred to single movements.

For example, looking left-to-right at row 1 in Table 1, in a load port process step, a wafer is picked-up by an LPR robotic mechanism (e.g., LPR-230) from the load port LPx and is placed at a following process module, chill plate CP1x (perhaps module 50 in Fig. 2). Transport time associated with picking-up and placing as shown in column 4 is 7.0 seconds. At row 2, a chill plate process step occurs for which the sum of process and overhead time is 24.0 seconds.

In the last column of row 2, a 20 second pre-planned wait time is added to the wafer process and overhead time, as described in U.S. patent no. 6,418,356.

The pre-planned wait times shown in the last column of Table 1 are determined and added to the wafer recipe process times before wafer production system 200 is even turned on. These are times added to non-critical module stages as described in the '356 patent to help resolve resource conflicts within track system 20'. These prior art "waits" are to be distinguished from "delays" that are added, as needed, during actual operation of wafer production system 200 to compensate for deviations from nominal periodicity within scanner system 30', according to the present invention.

After the expiration of the process, overhead and preplanned wait time at process module XP1x, a robotic mechanism CTR-230 takes 7.0 seconds to transport the wafer to the next process step, namely BARCx in row 3 of Table 1.

In row 3, a process and overhead time of 44.0 second is used for removal of the bead from the wafer circumferences, with a pre-planned wait of 33.5 seconds appended, according to the '356 patent. It is seen that a wafer swap robotic movement occurs in which 5.5 second transport time is used to move the wafer to the next process step, namely baking the wafer at hot plate HP1x in row 4 of Table 1.

Jumping down to shaded-rows 11-15, which involve process steps and robotic movements inside scanner system 30', an IN-PED step involves robotic mechanism SIR-230 placing a wafer on an input pedestal (IN-PED), the wafer having thus entered scanner system 30'. As indicated in Table 1, a wafer-handling robot (e.g, WHR-240) is then used to transport the wafer to the aligner stage (ALIGN), see exemplary system 200 shown in Fig. 2, and Table 1, row 12. Transport time is 12.5 seconds with 1.0 second process plus overhead time. Zero planned wait is required. At row 12 in Table 1, the wafer now undergoes an alignment step that involves 19.30 seconds process

plus overhead time, with 25.0 seconds pre-planned. The alignment takes place at a stage that is part of the DIR-240 robotic mechanism.

5 At the expiration of the alignment, overhead, and pre-planned wait time, the wafer in question now undergoes an exposure step that involves simply rotating the DIR-240 robot. Movement is such that one arm of the DIR-240 robotic unit holding an aligned wafer is rotated or moved into position to expose that wafer, while the other arm is free to move another wafer into the pre-alignment step. Table 1 indicates that the rotation takes 6.5 seconds
10 transport time, while 33.5 seconds are exposure plus overhead time, and zero seconds wait.

In the next row of Table 1, the WHR-240 robotic mechanism discharges the wafer from the exposure stage within scanner system 30' in 12.4 seconds with
15 1.0 seconds process and overhead time, and zero seconds wait. In row 15 of Table 1 (the last row directed to scanner system 30' per se) the SIR-230 robotic mechanism picks the wafer in question from the out pedestal (OUT-PED) associated with scanner system 30'. This maneuver takes nominally 9.5 seconds transport time with 1.0 seconds process and overhead time, with
20 zero seconds wait. The wafer has now completed processing within scanner system 30' and re-enters track system 20' as indicated in exemplary Fig. 2, for example beginning with a post-exposure bake step 90 (denoted as HP-3x in row 16 of Table 1).

25 Referring to Table 1, row 16, the wafer at hot plate HP3x undergoes 94.0 seconds of process plus overhead time in baking. DVR robotic mechanism 230 then picks and transports the wafer to chill plate CP3x in 7 seconds. The wafer then undergoes a chill plate process step, perhaps chill plate 100 in Fig. 2, denoted CP3x in Table 1. After 64.0 seconds of chill time plus overhead
30 time, robotic mechanism DVR-230 requires 5.5 seconds to transport the wafer to the developer module (see Table 1, row 18).

As shown in Fig. 2, typically the wafer next undergoes a developer step 110, denoted DEVx in Table 1, involving an 89.0 second process plus overhead time. In Table 1 the following step is another chill plate (CP4x), perhaps chill plate 50 in Fig. 2, after which the wafer exits track system 20' via a load port (denoted LPx in Table 1). It is understood that Fig. 2 and Table 1 are exemplary and indeed every step shown in Fig. 2 may not be reflected in Table 1.

Fig. 3 comprises Fig. 3A and Fig. 3B, the latter being a continuation of Fig. 3A. Figs. 3A and 3B graphically depict twenty-five wafers, denoted in the vertical axis as wafer number 1, ... 25, as the wafers undergo processing in system 200 as a function of elapsed time, shown on the horizontal axis. To reiterate, in the system described in U.S. patent no. 6,418,356, incorporated hereby by reference, various "wait" times were added to non-critical processes to avoid conflicts by different wafers for a common system resource, these waits being denoted as "planned waits" in the last column of Table 1. In Figs. 3A and 3B, such waits are shown as white bars, and are calculated for system 200' in Fig. 2 per the '356 patent. The legend of symbols on the right-hand portion of Figs. 3A and 3B identifies what the various rectangular and square-like symbols in Figs. 3A and 3B denote. Further, various exemplary regions of Figs. 3A and 3B are explicitly called out with identifying indicia at the top portions of Figs. 3A and 3B.

Fig. 4, comprising Figs. 4A-4F, is a spreadsheet showing the fabrication recipe for the twenty-five wafers in question. Figs. 3A and 3B graphically depict the data calculated and enumerated in detail in Figs. 4A-4F. As described herein, the various "wait" times shown in Figs. 4A-4F and depicted in Figs. 3A and 3B as white rectangles are wait times as described in the '356 patent, and are planned "waits" that are added to non-critical module stages to reduce problems associated with resource conflicts. By contrast, the

various inserted "delay" times shown in Figs. 4A-4F and depicted as black rectangles in Figs. 3A and 3B are time "delays" inserted according to the present invention to compensate for deviations from nominal timing (e.g., variability in scanner clock periodicity) in scanner system 30'. These delays
5 are added into system 200, depicted in Fig. 2.

In Fig. 4A, column 1 denotes wafer number (data for 25 wafers being shown in the column), and column 2 represents deviations (in seconds) from nominal 40.0 second timing or periodicity for scanner system 30', in the example being
10 described. It is these scanner system 30' deviations that are compensated for with inserted "delays", according to the present invention. The insertion of such "delays" advantageously helps to promote a better timing match between when track system 20' is ready to send a wafer into scanner system 30', and when scanner system 30' is ready to receive such a wafer, as well as
15 when scanner system 30' is ready to provide a wafer for further processing back into track system 20', and when track system 20' is ready to receive such wafer for further processing.

The interplay between Table 1, Figs. 4A-4F, and Figs. 3A and 3B will now be
20 described. Let us arbitrarily begin with wafer 4, which is the fourth wafer from the bottom in Fig. 3A. From the legend on the right portion of Fig. 3A we see that wafer 4 is completing its 49.0 second time in the CTx (coater module), some of the 49.0 seconds being to the left of Fig. 3A, e.g., not shown. The associated data appears in Fig. 4B, fourth row from top (e.g., data for wafer
25 4), column 26, CTx. Immediately after the CTX station, there is a 28.5 wait time, shown in Fig. 3A as a white bar commencing at about time 640 seconds, and denoted wait 6 in Fig. 4C, column 27, fourth row. Note in Fig. 4C, no insertion delay (as opposed to a "wait") is required, according to the present invention. Still looking at wafer 4 in Fig. 3A, after 28.5 seconds of wait time
30 has expired (at approximately 670 seconds along the time axis), the CTR-230

robot moves the wafer over a 5.5 second transport time (see Table 1; see Fig. 4C, row 4, column 29).

At about time 690 seconds wafer 4 is positioned on a hot plate HP2x for 94.0 seconds (see Table 1 and Fig. 4C, row 4, column 30). The end of the 94.0 second hot plate duration is approximately time 765 for wafer 4 in Fig. 3A. No additional wait, as disclosed in the '356 patent is required, as indicated by Fig. 4C, row 4, column 31, e.g., wait 7 is zero seconds.

Next as shown by the small rectangle in Fig. 3A that follows the relatively long hot plate rectangle symbol, the SIR-230 robotic unit takes wafer 4 for 7.0 seconds, reflecting data in Fig. 4C, at row 4, column 32. At about time 770 seconds, wafer 4 begins 64.0 seconds on cold plate CP2x (see Table 1, and Fig. 4C, row 4, column 33), as indicated by the rectangular bar in Fig. 3A that extends from about time 770 to about time 834. As shown by the white bar in Fig. 3A that follows, an intentional wait of 13.5 seconds is inserted (wait 8 in Fig. 4C, row 4, column 34), again as determined preferably following the disclosure in the '356 patent. Fig. 4C, row 4, column 35 shows that no delay per the present invention is required, e.g., delay 8 is zero. Next, as shown by the small rectangle beginning at about time 895 seconds, the wafer is moved by the SIR-230 robotic unit for about 5.5 seconds. The corresponding data appears in Fig. 4C, row 4, column 36, as well as Table 1.

As shown in Fig. 4C, row 4, column 37, no "delay" is inserted at this time, e.g., delay 9-10 is zero seconds. At about time 860 an OEBrx process step is carried out for 34.0 seconds, per Fig. 4C, row 4, column 38. In Fig. 3A, as shown by the small white rectangle, a wait of 5.0 seconds (wait 9 in Fig. 4C, row 4, column 39) follows. Immediately following is an inserted "delay" of 1.54 seconds, according to the present invention, denoted delay 11 in Fig. 4D, row 4, column 40. This delay is inserted at about time 895 in Fig. 3A. Next follows a robotic movement of wafer 4 with SIR 240 that occupies 8.0 seconds

(see Table 1, and Fig. 4D, row 4, column 41). The end of this 8.0 second movement occurs at approximately time 905 seconds in Fig. 3A.

5 Immediately following, wafer 4 spends zero time on the IN-PED station within scanner system 30' (Fig. 4D, row 4, column 42), and has zero inserted wait (Fig. 4D, row 4, column 43, e.g., wait 10 is zero). Wafer 4 is transported by WHR-240 (or equivalent) for 12.5 seconds (Table 1, Fig. 4D, row 4, column 44), for processing within scanner system 30'. In Fig. 3A, termination of this 12.5 second period occurs just before time 920 on the horizontal axis. From
10 Table 1 and Fig. 4D, row 4, column 45, an alignment step (ALIGN) follows for 19.3 seconds, which is followed in Fig. 3A by a white rectangle indicating a wait time of 25.0 seconds (Fig. 4D, row 4, column 46, denoted wait 11). In Fig. 3A, wait 11 ends just after time 960 seconds.

15 Thus just after about time 960 in Fig. 3A an intentional delay (delay 12 in Fig. 4D, row 4, column 47) of 1.86 seconds is added, according to the present invention. This delay is depicted as a narrow black rectangle in Fig. 3A. Next wafer 4 is moved by robotic unit DIR-240 over a 6.5 second transport time (see Table 1 and Fig. 4D, row 4, column 48). At about time 970 there is a
20 delay of 2.98 seconds (Fig. 4D, row 4, column 49). This is the delay in start-up of the exposure step, and it is this deviation or delay in nominal exposure starting time that the present invention compensates for (among other deviations). In Fig. 3A, exposure does not start until about time 975 seconds, and lasts for 33.5 seconds (see EXPOSE, Fig. 4D, row 4, column 50),
25 exposure shown as a solid rectangle that extends to about time 1008 seconds. No wait state is permitted after exposure (wait 12 is zero seconds in Fig. 4D, row 4, column 51).

Over a transport time of 6.5 seconds (see Table 1 and Fig. 4D, row 4, column
30 52), robotic unit DIR-240 moves wafer 4 to the discharge station (DISCHRG in Fig. 4E, row 4, column 53) for 1.0 second. No wait state is inserted (e.g., wait

13 is zero seconds per Fig. 4E, row 4, column 54). At about time 1015, robotic unit WHR-240 moves wafer 4 over a 12.4 second transport time (Table 1 and Fig. 4E, row 4, column 55) to the OUT-PED station in scanner system 30'. Per Fig. 4E, row 4, column 56, wafer 4 spends 1.0 seconds at this station, and is then moved by robotic unit SIR-230 with its 9.5 second transport time to hot plate HP3x, e.g., post-exposure bake module 90 in Fig. 2. Note from Fig. 4E, row 4, columns 57 and 58, that no wait time and no delay time is inserted (e.g., wait 14 is zero seconds, and delay 17 is zero seconds). The 9.5 second SIR-240 transport time is reflected in Table 1, and Fig. 4E, row 4, column 59.

As shown graphically in Fig. 3A by the hatched rectangle spanning from just before time 1040 through about time 1130, wafer 4 next remains on hot plate HP3x for 94.0 seconds (see Table 1 and Fig. 4E, row 4, column 60). No wait state is permitted after the post-exposure bake (e.g., Fig. 4E, row 4, column 61 shows wait 15 is zero seconds). Wafer 4 is immediately picked up by robotic unit DVR-230 and transported (with a 7 second transport time) to chill plate CP3x, e.g., module 100 in Fig. 2, for 64 seconds (see Table 1 and Fig. 4E, row 4, column 63). This 64 second wafer 4 cooling step commences in Fig. 3A at about time 1140 and extends off Fig. 3A to be terminated at the left edge of Fig. 3B, just after time 1200 seconds.

The white rectangle in Fig. 3B extending to about time 1215 seconds represents an inserted wait of 13.5 seconds (wait 16, Fig. 4E, row 4, column 64). Next follows an inserted delay of 5.03 seconds, according to the present invention, denoted delay 19 in Fig. 4E, row 4, column 65, and depicted as a dark rectangle in Fig. 3B, ending at about time 1220.

As suggested by Fig. 2, wafer 4 is next conveyed by robotic unit DVR-230 (with its 5.5 second transport time) to developer module 110 (or equivalent), for an 89.0 second development (see Table 1 and Fig. 4F, row 4, column 67).

This lengthy development process is shown in Fig. 3B as the long rectangle extending from about time 1220 to about time 1319 seconds. Looking at Fig. 4F, row 4, columns 68 and 69, wafer 4 is subjected to a 30.0 second wait (wait 17) and a 6.77 inserted delay (delay 20) before being transported by
5 robotic unit DVR-230. After the robotic transport time of 5.5 seconds (see Table 1 and Fig. 4F, row 4, column 70), wafer 4 is presented to a chill plate, e.g., module 50 (or equivalent) in Fig. 2, for 5.0 seconds (Table 1 and Fig. 4F, row 4, column 71). Again it is noted that Fig. 2 is generic and not every module depicted is necessarily reflected in the wafer recipe being described.

10 Wafer 4 is nearing the completion of processing. Per Fig. 4F, row 4, columns 72 and 73, wafer 4 undergoes a 31.0 second wait (wait 18), followed by a 2.45 second inserted delay (delay 21). In Fig. 4B, delay 21 terminates shortly before time 1400 seconds. Wafer 4 is then transported by robotic unit LPR-
15 230 (with 7 second transport time) to load port LPx of track system 20'. Wafer 4 is then pushed out of track system 20' slightly after time 1400 in Fig. 3B.

If we examine the other wafers shown in Figs. 3A and 3B, it is seen that at approximately every 40.0 seconds one of the twenty-five wafers to be
20 processed enters the system flow. As noted in column 2 in Fig. 4A, scanner time deviation from a nominal 40.0 second scanner clock period can vary from a nominal about 0 seconds to about 4.14 seconds. When computer system 210 detects such deviations from nominal scanner system time, an appropriate time delay is inserted into the system flow, as exemplified by Figs.
25 4A-4F.

It is the combination of pre-planned "wait states", as disclosed in the '356 patent, plus dynamically inserted "delays", according to the present invention, that promotes the desired synchronous wafer flow throughout scanner system
30 30' and track system 20', notwithstanding deviations in clock periodicity within scanner system 30'. For example, at about time 1217 seconds, dynamically

inserting delays to the movement of wafers 1 and 4 (Fig. 4F, row 1, column 69 and Fig. 4E, row 4, column 65) enables robotic unit DVR-230 to execute pick and placement of wafers 1, 4, and 7 in one continuous single-swap-swap motion.

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But for the insertion of these delays, according to the present invention, conflicts in the requests for pick and place by wafers 1, 4, and 7 would exist. Such conflicts would lead to the loss of synchronization of wafer flow across track system 20' and scanner system 30'. Examining Figs. 3A and 3B

10 vertically along various time instances, it is seen that resource conflicts are avoided as a result of the inserted wait states and time delays, notwithstanding perturbation in scanner periodicity. Determination of delay times, according to the present invention, may be carried out by software 220 using analytical techniques such as those disclosed in U.S. patent no.

15 6,418,356.

Although the exemplary system described assumed a 40 second period, which is to say a production of 90 wafers per minute, it will be appreciated that a faster throughput can also be implemented, for example at least 130 wafers

20 per minute, and preferably 160 wafers per minute.

Modifications and variations may be made to the disclosed embodiments without departing from the subject and spirit of the invention as defined by the following claims.

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